REMARKS

Claims 1-4, as amended, remain herein.

Claims 1-4 have been amended to recite more clearly simultaneously detecting (1) stuck-at failures and (2) short-circuited adjacent lines in the logic circuit.

Claims 1-4 also have been amended additionally to recite:

> extracting data representing input lines of a logic circuit of a semiconductor apparatus represented by layout data and identifying combinations of adjacent input lines of said input lines.

See applicant's Fig. 4 disclosing showing steps S201 and S202, wherein all input lines are identified and adjacent ones of such identified input lines are selected.

Claims 1-4 further recite:

> selecting one combination of adjacent input lines from said extracted combinations and setting each of said selected adjacent input lines to a first logical value of "0" or "1" (step S202 in Fig. 4) and setting said input lines other than the selected adjacent input lines to a second logical value of "0" or "1" (step S203 in Fig. 4), so that an expected logical output value is output by such logic circuit when a stuck-at failure and a short circuit between the adjacent lines do not exist and an unexpected output logical value is output when at least one of a stuck-at failure and a short circuit between the adjacent lines does exist (step S204 in Fig. 4).

See applicant's specification beginning at page 11, fourth paragraph, describing an example utilizing steps S201-S204, applied to an example circuit shown in Figs. 2 and 3, wherein logical values are set for adjacent lines and at the same time also for other input lines, such that the truth tables shown in Figs. 5(a)-5(c) are satisfied, so that both stuck-at failures and short-circuit failures are detected.

1. Claims 1-4 were rejected under 35 U.S.C. §103(a) over Endoh et al. U.S. Patent 5,485,094, Ferguson et al. U.S. Patent 6,202,181, and Parker et al. U.S. Patent 5,513,188. The claimed invention patentably defines over the references.

The presently claimed method (and related recording medium) for simultaneously detecting (1) stuck-at failures and (2) short-circuited adjacent lines in a logic circuit of a semiconductor apparatus includes selecting one combination of adjacent input lines from extracted combinations and setting each of selected adjacent input lines to a first logical value of "0" or "1" (step S202 in Fig. 4) and setting input lines other than the selected adjacent input lines to a second logical

value of "0" or "1" (step S203 in Fig. 4), so that an expected logical output value is output by such logic circuit when a stuck-at failure and a short circuit between the adjacent lines do not exist and an unexpected output logical value is output when at least one of a stuck-at failure and a short circuit between the adjacent lines does exist. This technique is nowhere disclosed or suggested in any of the cited references.

The presently claimed invention does not merely detect a short circuit between adjacent lines, but instead, expands the prior art inspection method for detecting stuck-at failures also to detect simultaneously a short circuit between adjacent lines by selecting (1) a set of adjacent input lines and (2) other input lines, and applying "1" or "0" logical values to all selected lines such that both stuck-at failures and short-circuited adjacent lines are simultaneously detected. See applicant's Figs. 5(a)-5(c) for truth tables showing an example of such combinations of selected lines and applied logical values, with reference to the example logic circuit shown in Figs. 1 and 2.

The Examiner asserts that a person skilled in the art would have modified the Endo '094 method for detecting stuck-at failures to include either of the Ferguson '181 and Parker '188 methods for detecting short-circuited terminals on the basis that all three references describe the importance of minimizing pattern selection to achieve faster testing. However, the teachings of such references are not properly combinable because neither Ferguson '181 nor Parker '188 teaches or suggests integrating their respective methods with any other method; while the desirability of faster testing is mentioned, the secondary references provide no guidance to a person skilled in the art to look in any particular direction, or give any clue about the kind of method that would be a candidate for being adapted to include the Ferguson '181 or Parker '188 steps. There is nothing in Ferguson '181 or Parker '188 that would motivate a person skilled in the art to identify and modify a method such as the Endo '094 method to reach the subject matter of claims 1-4.

Endo '094 allegedly discloses detecting stuck-at failures. But, as described in applicant's specification at page 4, lines

21-24, such prior art detection method gives the same outputted logical values for output terminals that are short-circuited as the outputted logical values for terminals that are not short-circuited, i.e., prior art stuck-at methods such as Endo '094 do not detect short-circuited output terminals. The Examiner admits that Endo '094 does not disclose or suggest extracting adjacent lines that may have a short circuit occurring between them (applicant's claims 1 and 3), wherein a distance therebetween is equal or less than a threshold distance (applicant's claims 2 and 4), and cites Ferguson '181 and Parker '188 as allegedly teaching same. More specifically, Endo '094 does not disclose or suggest detecting short-circuited output terminals, regardless of whether such terminals are related to adjacent lines.

Ferguson '181, while disclosing extracting adjacent lines, makes no mention of detecting stuck-at failures. Parker '188, disclosing setting a single bit to "1" and the rest to "0", and then cyclically moving such "1" amongst the other positions, does not teach selecting a set of inputs by focusing on adjacent

lines among the sets of inputs for detecting stuck-at failures, as presently claimed.

In contrast, applicant's claims recite applying a particular set of input values to a selected set of adjacent lines, together with applying another set of input values to other input lines in a way that results in detection of both stuck-at failures in the circuit and also any short-circuit between those adjacent, as recited in claims 1-4. There is nothing in the teachings of Ferguson '181 and Parker '188 that hints of a combined approach that replaces separate methods, one for detecting stuck-at failures and another for detecting short-circuits, with a dual-purpose method. Where, in Ferguson '181 and Parker '188, is there any indication that it would be beneficial or desirable to select two sets of input values, one to be applied to a combination of adjacent terminals and the other to be applied to some other selected set of input terminals for simultaneous testing for a short-circuit between adjacent lines and also stuck-at failures? Neither Ferguson '181 nor Parker '188 suggest going from each of their respective relatively simple single test method to a new combined-test

procedure, one that is far more complicated and that necessarily must be supported by a combined truth-table approach such as the example shown in applicant's Figs. 5(a)-5(c). Neither Ferguson '181 nor Parker '188 provide even the slightest hint of how to combine the logic underlying the Endo '094 short-circuit testing with the logic of the Ferguson '181 and Parker '188 stuck-at testing, to reach the invention of claims 1-4, or even to suggest that it would be desirable to do so.

For the foregoing reasons, none of Endoh '094, Ferguson '181 or Parker '188 contains any teaching, suggestion, reason, motivation or incentive that would have led one of ordinary skill in the art to applicant's claimed invention. Nor is there any disclosure or teaching in any of these references that would have suggested the desirability of combining any portions thereof effectively to suggest applicant's presently claimed invention. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

All claims 1-4 are now proper in form and patentably distinguished over all grounds of rejection stated in the Office Action. Accordingly, allowance of all claims 1-4 is respectfully requested.

Should the Examiner deem that any further action by the applicants would be desirable to place this application in even better condition for issue, the Examiner is requested to telephone applicant's undersigned representatives.

Respectfully submitted,

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